Amendments to Specification:

Please replace paragraph number [5], in its entirety, with the following paragraph:

[5] **Compaction** - Referring to **FIG. 2**, in semiconductor testing "compaction" is a technique used to reduce the number of output bits that need to be analyzed during a test function. The compactor ~~209~~ 9 consists of a number of serially connected cyclic shift register cells **CSRC** that form a cyclic shift register ~~212~~ 12. Typically, scan input data signals **SID** are shifted into a number of scan chains ~~210~~ 10 and then the scan output data signals **SOD** from these scan chains are gated with compactor feedback data signals **CFD** from the cyclic shift register cells **CSRC**. Each cyclic shift register cell **CSRC** receives gated input from an XOR gate ~~211~~ 11. When all the scan output data has been shifted through the cyclic shift register ~~212~~ 12, the value retained in the cyclic shift register has a known value which can be shifted out and analyzed as a compacted output data signal **COD**. For example, one can shift in 1000 bits through the cyclic shift register ~~212~~ 12 that may only have 20 cyclic shift register cells **CSRC**. Therefore, instead of having to analyze and compare all 1000 bits to a known bit pattern, one only need compare the final 20 bits from the compaction cyclic shift register ~~212~~ 12 to the known bit pattern.

Please replace paragraph number [6], in its entirety, with the following paragraph:

[6] Referring again to **FIG. 2**, although not a problem per se with compaction, much of the data that is input to the compaction cyclic shift register ~~212~~ 12 is of a don't care nature. That is, some of the compacted output data **COD** is non-deterministic meaning that one cannot predict its value based on the value of the scan output data signal **SOD**. Therefore, in order to allow compaction to work, *i.e.*, so that an unknown value doesn't give an unknown result, the don't care

data values need to be masked. Referring to **FIG. 3**, this is done with logic for each individual cell **17** of the cyclic shift register ~~212~~ 12 **(FIG.2)** that is adjacent to and part of the same circuit as the cyclic shift register. The mask signal **13** and the scan output data **SOD** are gated with an AND gate **15** before being input to the individual cell **17**. By changing the value of the mask signal **13**, one can mask the scan output data **SOD** for a given clock cycle. Consequently, the output **18** of the individual cell **17**, is no longer of a don't care nature.

Please replace paragraph number [34], in its entirety, with the following paragraph:

[34] Still referring to **FIG. 8**, the control signals **70** are for scan output **71**, select scan **72** and sample output control **73**. These controls are input to an AND gate **74** and provide control input based on tester settings to an ~~OR~~ XOR gate **81** that then gates the VP flip-flop **54**. The AND gate **80** provides an output signal to the ~~OR~~ XOR gate **81** and then an input to the VP flip-flop **54** when not in compact mode. AND gate **80** has four input signals, output enable **75**, not-scan **76**, output data **77,** and sample output control **73**.

Please replace paragraph number [38], in its entirety, with the following paragraph:

[38] Therefore, referring to **FIG. 10**, an embodiment of input/output circuitry **106** that uses two flip-flops is shown, according to an embodiment of the invention. The reseed flip-flop **87** and associated reseed circuitry **86** is used for the reseed built in self-test function, while the compaction flip-flop **102** and associated compaction circuitry **99** is used for compaction. As shown, the reseed flip-flop **87** need not be coupled to the I/O pin **31**, and can therefore be connected to the scan input **93** via multiplexer **92**. The reseed circuitry **86** is similar to that described in **FIG. 9** above. The input signal **90** is inverted **89** and

multiplexed **92** with the reseed flip-flop output **88**. The multiplexer **92** is controlled by the LFSR enable control signal **91**. A reseed multiplexer **95** is controlled by a reseed enable control signal **94** and multiplexes the scan input data **93** with the output of an ~~or~~ XOR gate **96**, which has inputs LFSR-input **97** and LFSR-feedback **98**.